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PATENT

Attorney Docket No. 012172-005010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Howard G. Sachs, et al.

Serial No.: 08/422,753

Filed: April 13, 1995

For: SOFTWARE SCHEDULED
SUPERSCALER COMPUTER
ARCHITECTURE

Examiner: V. Darbe

Art Unit: ~~2345~~

2318

PRELIMINARY AMENDMENT

#14/c
LDS
8-2-95
entered

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Examiner:

Before examination on the merits, please amend the above-identified application as follows:

In the Claims:

Please amend claims 1-23 as follows. Claims 1-23 as presently amended are presented in Appendix A for ease of reference:

1. (Amended) A computing system having a plurality of processing pipelines for executing [a group] groups of individual instructions, within very long instruction words [in parallel], each [of the] individual [instructions] instruction to be executed in [a] each group being executed by [a] different processing [pipeline] pipelines in parallel, the computing system comprising:
- a main memory for storing a very long instruction word;